ARM SINGLE-CYCLE CPU

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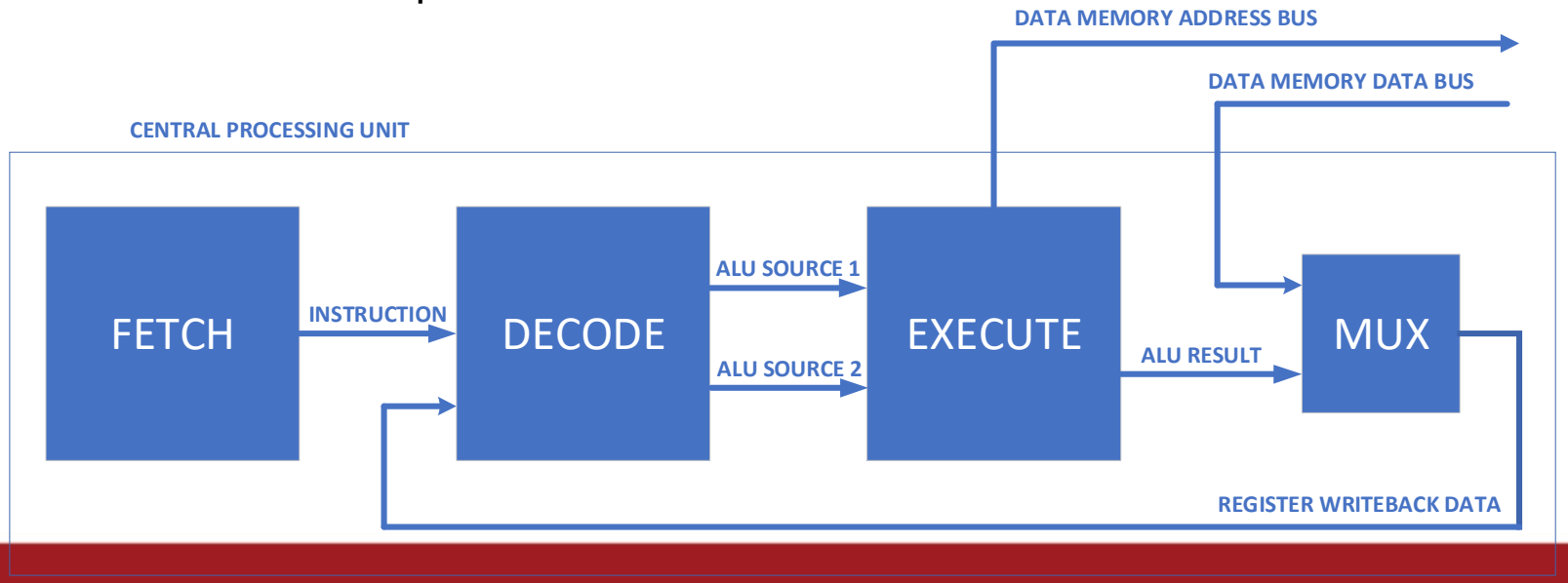
CENTRAL PROCESSING UNIT CIRCUITRY

- The CPU circuit can be divided into three phases
  - **Fetch** retrieves the instruction to execute from instruction memory.
  - **Decode** retrieves the ALU source data and sets control signals.
  - **Execute** completes the instruction arithmetic.



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IMPLEMENTING THE MICROARCHITECTURE

- Register transfer equations guide the design
  - **Arithmetic flow** equations describe the calculation.
  - **Control flow** equations describe the program counter change.
  - **Common items** reflect direct connections while **choices** reflect multiplexers.

TYPE	ARITHMETIC FLOW EQUATION	CONTROL FLOW EQUATION
Data Processing R	R[Rd] ← R[Rn] op R[rm]	PC ← PC+4
Data Processing I	R[Rd] ← R[Rn] op imm32	PC ← PC+4
Load Register	R[Rd] ← M[R[Rn]+imm32]	PC ← PC+4
Store Register	M[R[Rn]+imm32] ← R[Rd]	PC ← PC+4
BEQ		PC ← BrAddr if Z=1 else PC ← PC+4
BNE		PC ← BrAddr if Z=0 else PC ← PC+4

IMPLEMENTING THE MICROARCHITECTURE

- Destination register is always specified R[Rd].
- ALU Source 1 is always R[Rn].
- ALU Source 2 is either R[Rm] or the extended and rotated immediate: MUX
- PC is either PC+4 or the branch address: MUX

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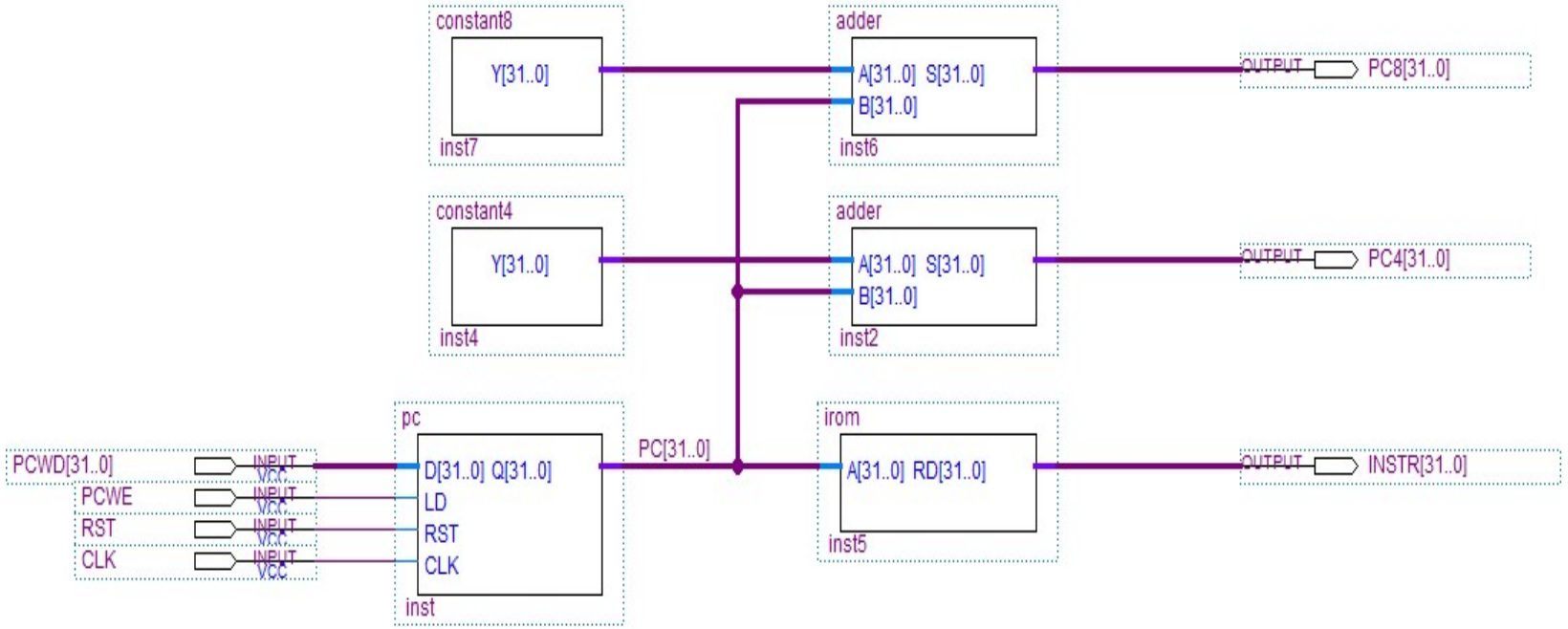
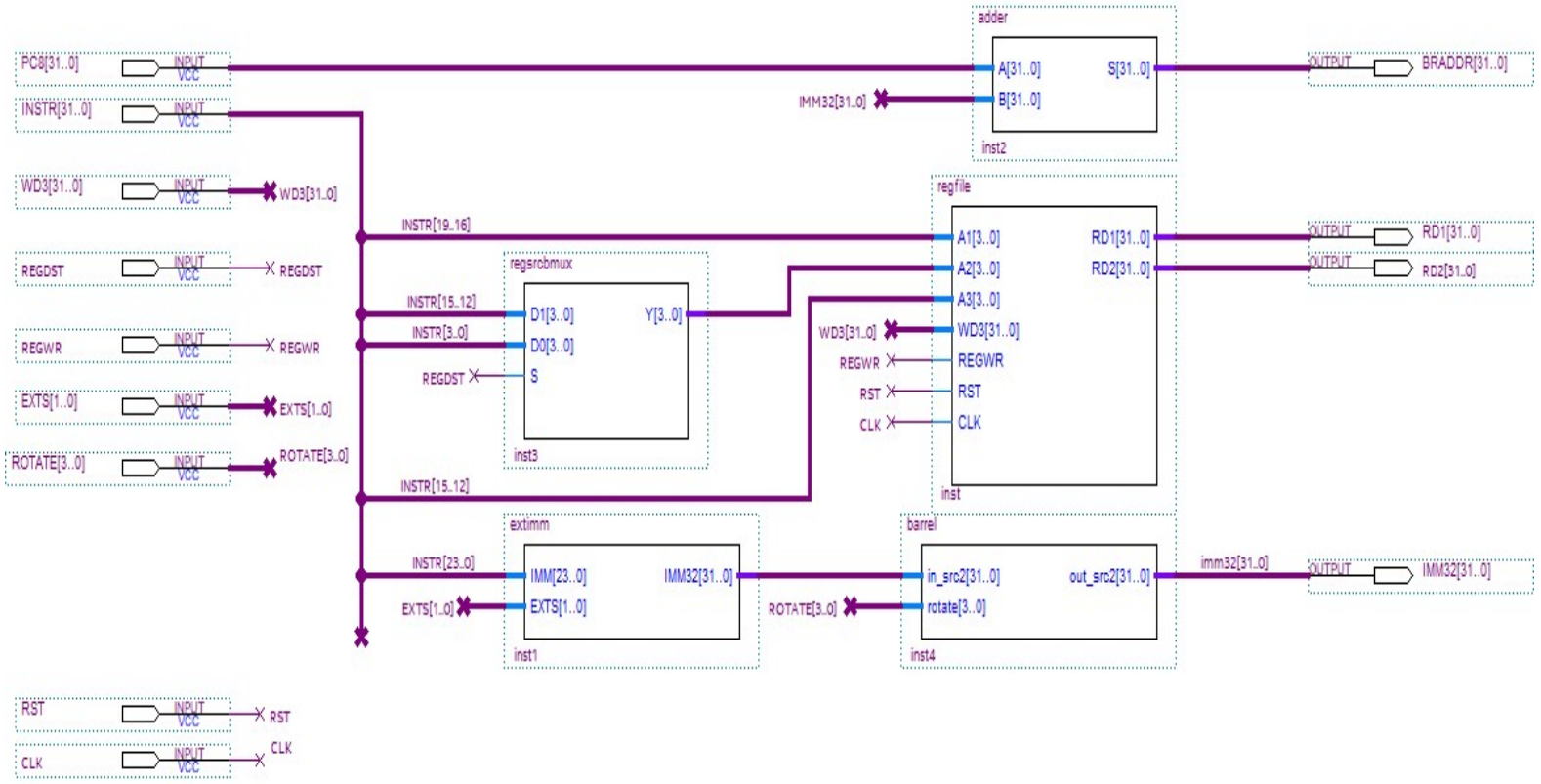
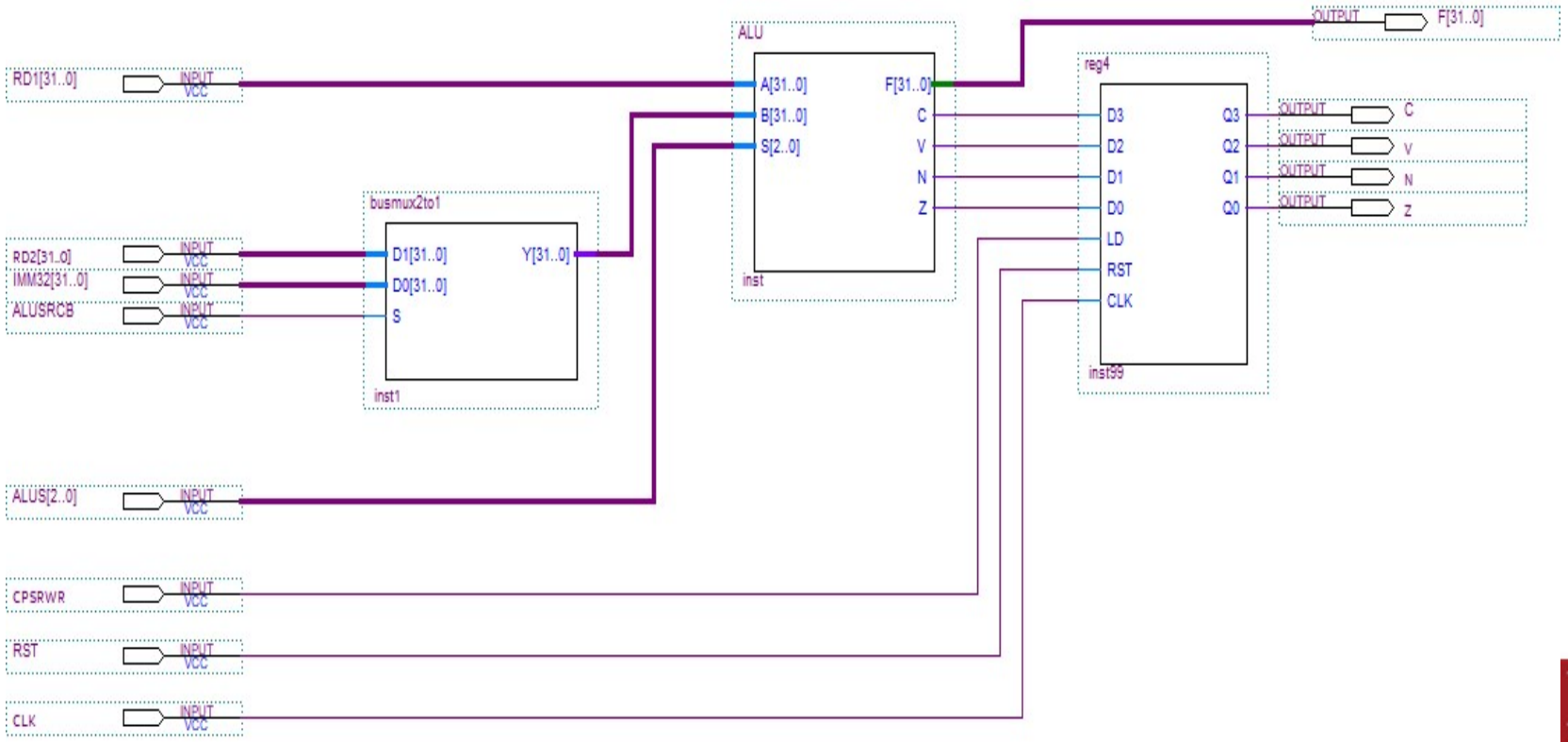
IMPLEMENTING THE FETCH CIRCUIT



IMPLEMENTING THE DECODE CIRCUIT



IMPLEMENTING THE EXECUTE CIRCUIT



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IMPLEMENTING THE COMPUTER